# MEMORY DEVICES WITH SELECTIVELY ENABLED OUTPUT CIRCUITS FOR TEST MODE AND METHOD OF TESTING THE SAME


## ABSTRACT OF THE DISCLOSURE

A memory device, such as a DDR SDRAM, may be provided in which subsets of data output circuits of the device can be selectively enabled to allow sets of data output pins to be connected in common in a testing configuration. In some embodiments, a memory device includes a plurality of data output circuits, respective ones of which are configured to receive data from respective internal data lines and respective ones of which are coupled to respective data input/output pins. The device further includes a data output control circuit operative to selectively enable subsets of the plurality of data output circuits to drive their respective corresponding data input/output pins responsive to an externally-applied control signal. The data output control circuit may be operative to selectively cause subsets of the plurality of data output circuits to present a high impedance at their respective corresponding data input/output pins. The invention may be embodied as devices and methods.